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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/090,348	03/04/2002	Friedrich Hapke	PHDE 010056	3969

24737 7590 09/15/2003

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER
HOLLINGTON, JERMELE M

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 09/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/090,348	HAPKE, FRIEDRICH	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,8 and 10* is/are rejected.

7)☒ Claim(s) *5,6 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *27 June 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings were received on June 27, 2003. These drawings are approved.

Claim Objections

2. Claim 4 is objected to because of the following informalities: in line 2 of the claim, it appears that a phrase or words are missing between "logic circuit" and "the effect." Currently, the examiner is unable to understand "...wherein there is provide a masking logic circuit the effect of which is that..." Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4. Claims 3 and 5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 3, the claim recites, "...means for test pattern generation is a bit flipping controller which controls bit flipping logic circuits..." The specification does not particularly point out that the means for test pattern generation is a bit-flipping controller as claimed. In claim 1, which claim 3 depends off of, it states: "...means for test pattern generation, which modify the deterministic data words such that prescribed, deterministic test patterns which can be fed to inputs of the integrated circuit..." On page 5, lines 8-9, it states: "...the bit flipping logic circuits 3, 4, and 5 are to supply a data word which fed to the inputs of the IC to be tested.

For examination purposes, the examiner is taking a position that the means for test pattern generation is the bit-flipping logic circuit and not the bit-flipping controller as claimed. Since claim 5 depends off of claim 3, it is also rejected for the above reason.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4, 7-8 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Ando (4710704).

Regarding claims 1 and 10, Ando discloses an arrangement (see Fig. 2) for testing an integrated circuit (IUT 22), the arrangement comprising a data word generator (control signal generator 29), which supplies deterministic data words, means (terminals 31, 33 and 35) for test pattern generation, which modify the deterministic data words such that prescribed, deterministic test patterns which can be fed to inputs of the integrated circuit (22) to be tested, are produced, and comparison means (comparator 53) for comparing test output patterns of the integrated circuit (22) with at least one desired output pattern, the arrangement being provided outside the integrated circuit (22) to be tested.

Regarding claim 2, Ando discloses a feedback shift register is provided as the data word generator (31, 33 and 35).

Regarding claim 3, Ando discloses means (31, 33 and 35) for test pattern generation is a bit flipping logic circuits which is being controlled by bit flipping controller (test pattern

generator 21) such that the deterministic data words are modified in a bit wise fashion such that the prescribed, deterministic test patterns are produced.

Regarding claim 4, Ando discloses a masking logic circuit (switch control circuit 36) wherein the comparison means (53) exclusively compare prescribed test output patterns of the integrated circuit (22) to be tested with the desired output patterns.

Regarding claim 7, Ando discloses the desired output pattern is generated by means of the data word generator (29) and with means (31, 33 and 35) for test pattern generation.

Regarding claim 8, Ando discloses the arrangement is implemented as a programmable logic circuit.

Conclusion

7. Claims 5-6 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: regarding claim 5, in the examiner's opinion, it would not have been obvious to a person of ordinary skill in the art to provide a test pattern counter that supplies the counting result to the bit flipping controller and/or the masking logic circuit in combination with the apparatus provide by Ando.

Regarding claim 6, in the examiner's opinion, it would not have been obvious to a person

of ordinary skill in the art to provide a signature register, which logically intercombines consecutive test output patterns, in combination with the apparatus provide by Ando.

Regarding claim 9, it would not have been obvious to a person of ordinary skill in the art to provide a test board (35), which is connected between a test system (23) and the IC to be tested in combination with the apparatus provide by Ando.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Heybruck (5488612), Crouch et al (5617531), Slizynski et al (6057679), Lee et al (6411124), Baker (EP164209A1) and Hapke (JP2002333466A) disclose a method and apparatus for testing integrated circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (703) 305-1653. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (703) 308-1233. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Jermele M. Hollington
Examiner
Art Unit 2829

JMH
September 3, 2003

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
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